REMARKS

The Examiner is thanked for the thorough examination of this application. The Office Action, however, tentatively rejected claims 1-15. The Office Action objected to claims 1 and 10 for containing the word "proving" instead of "providing." Applicant has amended these claims to correct this language, and therefore overcome this objection. Applicant has also canceled claims 16-22.

In addition, claims 1-8, 10, and 12-15 stand rejected under 35 U.S.C. 102 (e) as allegedly anticipated by Perng et al (US 2002/6498067). Claims 5, 9 and 11 stand rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Perng et al (US 2002/6498067), and further in view of Sechugraf et al (US20006140203) and Samavedam et al (US20026423632). Reconsideration of these rejections is respectfully requested in light of the remarks set forth below.

Rejections under 35 U.S.C. 102(e)

Applicant respectfully traverses the rejections made by the examiner for the reason discussed below.

Claim 1 recites:

> 1. A method of forming an integrated circuit transistor, comprising:
> providing a semiconductor substrate with a gate structure formed thereon;
> forming at least one dielectric layer overlying the semiconductor substrate, wherein the at least one dielectric layer comprises at least one first portion along at least one sidewall of the gate structure, and at least one second portion outside the gate structure along the surface of the semiconductor substrate;
> ***forming at least one first doped region*** in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one dielectric layer, ***wherein the at least one second portion of the at least one dielectric layer remains overlying the at least one first doped region***;

forming a sidewall spacer overlying the at least one dielectric layer along the at least one sidewall of the gate structure; and

forming at least one second doped region in the semiconductor substrate laterally adjacent to the sidewall spacer.

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose those features emphasized above.

Likewise, claim 10 recites:

10. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate with a gate structure formed thereon;

blanket depositing at least one first dielectric layer overlying the semiconductor substrate without performing an etch process on the at least one first dielectric layer;

wherein, the at least one first dielectric layer comprises at least one first portion along at least one sidewall of the gate structure;

wherein, the at least one first dielectric layer comprises at least one second portion outside the gate structure along the surface of the semiconductor substrate; and

performing a first ion implantation process to form at least one first doped region in the semiconductor substrate laterally adjacent to the at least one first portion of the at least one first dielectric layer, ***wherein the at least one second portion of the at least one first dielectric layer remains overlying the at least one first doped region***.

(*Emphasis added.*) Claim 10 patently defines over the cited art for at least the reason that the cited art fails to disclose those features emphasized above.

Accordingly, the express claim language of independent claims 1 and 10 requires the second portion of the dielectric layer to remain overlying the first doped region when forming the first doped region. In this regard, Fig. 2A to 2B, and page 10-13 of the presently application provides that the LDD region 50 is formed ***after*** the formation of the first dielectric layer 46 on the gate conductive layer 44 and the gate dielectric layer 42 by a blanket deposition. In addition, the first portion 46a of the first dielectric layer 46 covering the sidewalls of the gate conductive layer 44 serves as an offset spacer for the LDD ion implantation process. The second portion 46b

of the first dielectric layer 44 overlying the substrate serves as an out-diffusion stop layer to protect the semiconductor substrate 40 from surface damage during LDD ion implantation process 48.

In contrast, the cited reference does not teach or suggest forming a dielectric layer overlying the gate structure and the substrate before the formation of LDD region. To the contrary, in Perng's process, the first insulating layer 5 is formed on the sides of gate structure 3 after the formation the LDD region 4 in the semiconductor substrate 1. In other words, during the LDD ion implantation process, there is no dielectric layer on the sidewall of the gate structure 3 to serve as a spacer for lowering the capacitance between the gate conductive layer and the LDD region, and no dielectric layer overlying the semiconductor substrate 1 to protect the surface thereof from damage during the LDD ion implantation process. (See Fig. 1 to Fig. 2 and column 3 of Perng et al.) Indeed, Perng fails to teach or suggest a dielectric layer overlying the semiconductor substrate during the formation of LDD region in the substrate, as defined in the claimed embodiments of the present application.

For at least this reason, independent claims 1 and 10 are novel and non-obvious over the cited reference. Insofar as claims 2-8 and 12-15 depend from claim 1 and 10, these claims are also allowable at least by virtue of their dependency.

Rejection under 35 U.S.C. 103(a)

Claims 5, 9, and 11 stand rejected under 35 U.S.C 103(a) as allegedly unpatentable over Perng et al (US 2002/6498067), and further in view of Sechugraf et al (US20006140203) and Samavedam et al (US20026423632).

Claims 5, 9, and 11 ultimately depend from independent claims that include the aforementioned elements that are novel and non-obvious over the cited art, and thus these claims are also in condition for allowance for at least that reason.

As a separate and independent basis for the patentability of claims 5, 9, and 11, Applicant respectfully submits that the Office Action has failed to cite a proper suggestion or motivation for combining the three references. In combining Samavedam with Perng, the Office Action stated only that it would have been obvious "because TEOS can be use to isolation of gate in the semiconductor transistors." (Office Action, p. 8). In combining Schuegraf with Perng, the Office Action alleged that it would have been obvious "because TEOS density can be also characterized relative to an etch rate of about 175 Angstroms/minute." (Office Action, p. 9). These alleged motivations are clearly improper in view of well-established Federal Circuit precedent.

It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. *W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc.*, 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicant nots that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. *Stiftung v. Renishaw PLC*, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a sidewall spacer as claimed by the Applicant.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. *See In re Dembiczak*, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "clear and particular." *Dembiczak*, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. *See In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *Gambro*

Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. *Winner Int'l Royalty Corp. v. Wang*, No 98-1553 (Fed. Cir. January 27, 2000).

Although the suggestion to combine references may flow from the nature of the problem, see *Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.*, 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630 (Fed.Cir.1996), "[d]efining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness," *Monarch Knitting Mach. Corp. v. Sulzer Morat Gmbh*, 139 F.3d 877, 880, 45 USPQ2d 1977, 1981 (Fed.Cir.1998). Therefore, "[w]hen determining the patentability of a claimed invention which combines two known elements, 'the question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination.' " *In re Beattie*, 974 F.2d 1309, 1311-12, 24 USPQ2d 1040, 1042 (Fed.Cir.1992) (quoting *Lindemann*, 730 F.2d at 1462, 221 USPQ at 488).

The alleged motivations are simply insufficient and improper in view of the above-discussed Federal Circuit precedent.

For at least the foregoing reasons, all claims 1-15 are believed to be in condition for allowance, and the Examiner is respectfully requested to pass those claims to issuance. If the Examiner believes a teleconference will expedite the examination of this application, the Examiner is invited to contact the undersigned attorney at 770-933-9500.

No fee is believed to be due in connection with this Amendment and Response to Office Action. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to deposit account 20-0778.

Respectfully submitted ,

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